ABSTRACT

A semiconductor storage device is provided in which a plurality of word lines are activated together by causing each of the word lines which is once activated to hold the activated state during a plurality of successive word line selection cycles. The semiconductor storage device includes a latch circuit. The latch circuit derives the logical AND of a signal activated when a corresponding memory block is accessed and a redundancy miss is first made and a signal generated in each cycle to determine timing for activating a sense amplifier in each cycle, and generates and holds a sense amplifier activation signal.